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Paper title High radix booth MAC unit using prefix topology for low complexity DSP applications.

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Abstract: *This paper, for the first time, we present prefixes topology based accumulation units with variable latency to link equations via parallel-prefix computation using various methodologies such as such as ripple carry adder, Kogge Stone adder, Brent Kung adder, Ladner Fischer adder and Han Carlson adder. This work is also permitted to design high-speed and unique MAC hardware structure using vedic multiplier, thereby making them suitable for any DSP applications. To prove the hardware efficiency of the Wallace tree multiplier unit it is compared with state-of-the-art methods like high speed vedic and shift and add based DA method. Moreover, this methodology has several attractive features such as simplicity, regularity and modularity of architecture. Also, the booth radix-8 technique can be designed to meet high speed demand requirements of FIR filter design, where all bits of one tap unit are processed within the bounded delay. To reduce the complexity of filter, coefficients are represented in canonical signed digit representation as it is more efficient than traditional binary representation. The comparative analyzes is carried out using 20 order FIR filter. Hardware optimization in terms of area, delay and power of different prefix techniques, Vedic multiplier, add and shift method and Wallace tree (WT) multiplier are is analyzed using FPGA hardware synthesis. Finally performance efficiency of FIR filter design is proved using ECG signal de-noising application.*
Keywords: *prefix adder, MAC, FIR design, DSP etc.*

I. Introduction

High speed MAC units are inevitable in many real time applications like filter design, image processing, data acquisition and control [1]–[2]. In particular Digital Signal Processing (DSP) requires custom accelerators to perform computationally intensive arithmetic's. Typical DSP applications need to carry out a large number of MAC operations as their implementation is based on multiplier kernels. As expected, the overall system performance of DSP systems is considerably affected by both hardware complexity latency measures. It is investigated in many existing research works as arithmetic optimization models [3] have concludes that the design requires both high speed operations with significant improvements in complexity reduction.

Though multiplier is major hardware and power hungry digital blocks in most signals and image processing systems such as FIR filters, digital signal processor, microprocessors etc its metrics also depends on accumulation units. With advances prefix topology, many researchers have tried and strive the efficiency of MAC design which offers either of the following- high speed, low power consumption or more considerably less hardware combination, thus making them compatible for various high speed, low power, and compact VLSI implementations. However, area and speed are opposite conflicting constraints. Therefore, improving speed always results in larger area. The most efficient multiplier structure will vary depending on the throughput requirement of the application. The first step of the design process is the selection of the optimum circuit structure. There are various structures to perform the multiplication operation starting from the simple serial multipliers to the complex parallel multipliers.

Optimization of hardware complexity, speed and energy efficiency of digital MAC and its analogue DSP blocks becomes a challenging task with increase in digital components [4, 5]. One such application is designing MAC for FIR filter, which further complicates the worst case delay propagation situation with increased design complexity over its filter order [6]. Many previous works [7, 8] have focused on hardware efficient implementation of FIR filters using various adders and multipliers and also using some DA models like canonical sign digit representation of filter co-efficient. Similarly, a hardware sharing multiplication approach [9] which is a combination of add and shift operations over the common computation results has also been implemented earlier. However, the major problem with this sharing multiplication method is that, as the number of bits used to represent filter coefficients significantly increase, an additional large memory area will be needed

for computation sharing. Therefore, in the present work we prefer the multiplication using add and shift method with canonical signed digit (CSD) representation.

II. Mac Unit

2.1 Prefix Algorithms

Two categories of prefix algorithms can be distinguished; the serial prefix, and the tree-prefix algorithms. Tree-prefix algorithms include parallelism for calculation speed-up, and therefore form the category of parallel-prefix algorithms. Equation 3.21 represents a serial algorithm for solving the prefix problem. The serial-prefix algorithm needs a minimal number of binary • operations and is inherently slow (O(n)).

According to equation 3.20, all outputs can be computed separately and in parallel. By arranging the operations • in a tree structure, the computation time for each output can be reduced to O(log n). However, the overall number of operations • to be evaluated and with that the hardware costs grow with (O(n2)) if individual evaluation trees are used for each output.

As a tradeoff, the individual output evaluation trees can be merged (i.e., common sub-expressions be shared) to a certain degree according to different tree-prefix algorithms, reducing the area complexity to O(n log n) or even O(n). Binary addition has been presented as a prefix computation next. The prefix problem of binary carry-propagate addition computes the generation and propagation of carry signals. The corresponding to the bit generates gi and bit propagate pi signals have to be computed from the addition input operands in a pre processing step.

III. Booth Recoding

In the modern world, we need system which will run at high speed. Multipliers play an important part in today's DSP and DIP applications. In many cases for image processing applications multiplications are used larger in number. Therefore, speed improvement in multiplier is important. Advances in technology have permitted many researchers to design multipliers which offer both high-speed and unique hardware structure, thereby making them suitable for specific VLSI implementation.

In any multiplication algorithm, the multiplication operation is carried out by summation of decomposed partial products. For high-speed multiplication we need to apply a booth radix recoding multiplication algorithm. In recent days in all high radix booth algorithm recoding is changed from 2s-complement format to a signed-digit representation from the defined set. This is called modified booth algorithm.

3.1 Radix-8 Algorithm

Here we reduce the number of partial products using a higher radix in the multiplier recoding. Recoding of binary numbers was first invented by Booth [5]. The modified Booth's algorithm is done by appending a zero to the right of M. Figure 2 shows recoding of 01010001$_2$. In radix-8 recoding is similar to radix-4 [6] but here we take four bits instead of three bits and then we represent that coded values in signed-digit representation using Table 1.

Dk D2 D1

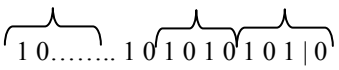

Fig. 1: Recoding representation

Where k is the number of partial products to be generated.

Table 1. Radix-8 Sign Digit Values

Coded bits	signed-digit value
0000	0
0001	+1
0010	+1
0011	+2
0100	+2
0101	+3
0110	+3
0111	+4
1000	-4
1001	-3
1010	-3
1011	-2

1100	-2
1101	-1
1110	-1
1111	0

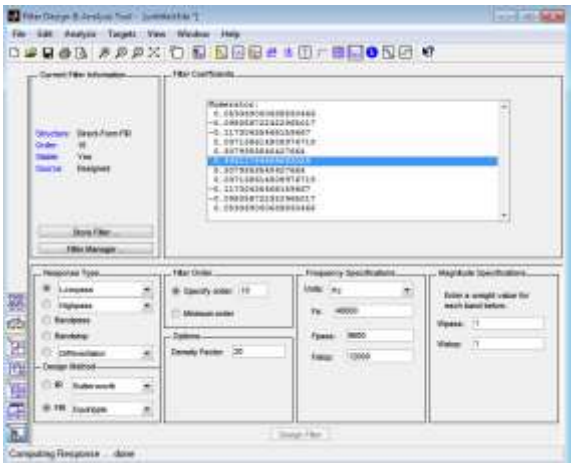

Fig.2: Filter coefficient extraction using FDA tool

IV. Fir –Denoing Application

Here low pass FIR filter coefficient generation is carried out using FDA filter design analyzer tool and preprocessed successfully using MATLAB. And ECG signal is also generated and converted into 2's complement representation and these digital values are stored as a text file using block RAM. Memory unit basically consists of two units: 1) pre-processed FIR coefficients; 2) Noisy ECG signal component;

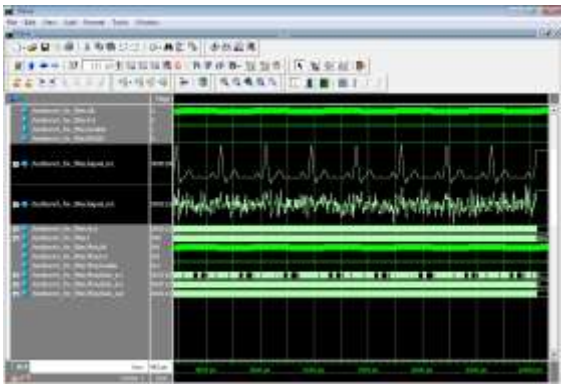

Fig.3: FIR filters simulation for ECG de noising.

V. Experimental Results

Here we compare the performance and speed trade off over area constrains of various MAC units using compound prefix adder with existing well known benchmark multiplication schemes which explored in table 1 and 2 with the schemes described in section 1. We extended this analyzes using FIR filter implementation schemes and implemented them for DSP applications as ECG signal de-noising. The hardware synthesis was carried without to prove the core objective of this work with improved performance report of the aforementioned designs, and its metrics over architectural level modifications and also the highest achievable complexity reduction and frequency.

Table 2 Trade off measures of prefix methodologies

Adder type	AREA	Fmax report
FIR MUL - Brent Kung	426	244.32 MHz
FIR MUL - Han Carlson	243	116.01 MHz
FIR MUL - Kogge stone	748	234.3 MHz
FIR MUL - Ladner Fischer	438	310.95 MHz

Table 3 Trade off Trade off measures of various MAC units

Multiplier type	AREA	Fmax report
FIR MUL – Wallace tree	1591	268.46 MHz
FIR MUL - Vedic	664	83.13 MHz
FIR MUL – shift/add	859	307.03 MHz
FIR MUL - CSD	601	131.98 MHz

Here FIR MAC designs are synthesized to ALTERA cyclone III FPGA using Quartus II tool. Our booth recoded consumes 28.85% and 39.40% lower than the existing methods. Our design also has a critical path delay of 1.35ns, which is several times faster than all other existing MAC types. The efficiency could be consistent with nominal higher bit width operands. As it stands, the performance metrics of proposed bit serial shift-add based MAC network makes it a prerogative choice for DSP application.

VI. Conclusion

In this paper we prove the efficiency of parallel prefix technique based adder unit and high speed vedic and wallace multiplier unit based FIR design over all other efficient multiplier less FIR filters. First, we compare the low cost proposed DA based algorithm with maximum adder depth followed by the CSD based thresholds of FIR coefficients. To extend the proposed DA based model that combines shifting and adding techniques to carried out FIR filtering in ECG signal denoisng applications. The effectiveness of our improved booth recoded MAC is verified using FIR implementation unit. And finally the complete trade of metrics of booth encoded multiplier unit with prefix topology based accumulation unit is validated using hardware synthesis.

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